# Monday, October 8th

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| 8.30-9.00 | **Registration** | |
| 9.00-9.30 | **Opening session**<br>Room: Sala Mascagni | |
| 9.30-10.30 | **Keynote** - Giovanni De Micheli (EPFL Switzerland): Cyber-Medical systems: requirements, components, design<br>*Chair: Dominique Borrione (Univ. Grenoble-Alpes, France)*<br>Room: Sala Mascagni | |
| 10.30-11.00 | Coffee break | |
| 11.00-12.20 | **Session 1**: Emerging technologies and computing paradigms<br>*Chair: Andrea Calimera (Politecnico di Torino, Italy)*<br>Room: Sala Mascagni | **Special session 1**: IoT for health, wellness and personal assistance<br>*Chair: Daniel Chillet (IRISA, France)*<br>Room: Sala Ponchielli |
| | 11.00 - *Swagata Mandal, Debjyoti Bhattacharjee, Yaswanth Tavva and Anupam Chattopadhyay:* **ReRAM-based In-Memory Computation of Galois Field Arithmetic**<br>11.20 - *Md Adnan Zaman and Srinivas Katkoori:* **Minimizing Performance and Energy Overheads Due to Fanout In Memristor based Logic Implementations**<br>11.40 - *Juinn-Dar Huang, Chia-Hung Liu and Wei-Hao Yang:* **Versatile Ring-Based Architecture and Synthesis Flow for General-Purpose Digital Microfluidic Biochips**<br>12.00 - *Francesco Barchi, Gianvito Urgese, Andrea Acquaviva and Enrico Macii:* **Directed Graph Placement for SNN simulation into a multi-core GALS architecture** | 11.00 - *Reza Ranjandish and Alexandre Schmid:* **Implantable IoT System for Closed-Loop Epilepsy Control based on Electrical Neuromodulation**<br>11.20 - *Marc Souchaud, Pierre Jacob, Camille Simon-Chane, Aymeric Histace, Maurice Tchuenté and Denis Sereno:* **Mobile Phones Hematophagous Diptera Surveillance in the field using Deep Learning and Wing Interference Patterns**<br>11.40 - *Julien LeKernec, Francesco Fioranelli, Shufan Yang, Jordane Lorandel and Olivier Romain:* **Radar for assisted living in the context of Internet of Things for Health and beyond**<br>12.00 - *Achraf Lamlih, Philippe Freitas, Mohamed-Moez Belhaj, Vincent Kerzerho, Fabien Soulier, Serge Bernard, Tristan Rouyer, Sylvain Bonhommeau and Jérémie Salles:* **A Hybrid Bioimpedance Spectroscopy Architecture for a Wide Frequency Exploration of Tissue Electrical Properties** |
| 12.20-13.30 | Lunch | |
| 13.30-14.30 | **Keynote** - Yervant Zorian (Synopsys, USA): Test & reliability challenges in the internet of things<br>*Chair: Franco Fummi (Univ. Verona)*<br>Room: Sala Mascagni | |
| 14.30-16.00 | PhD forum<br>*Chair: Sara Vinco (Politecnico di Torino, Italy)*<br>Room: Sala Mascagni (2-slide presentation); Foyer (Posters) | |

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| | *Vojtech Mrazek:* **Evolutionary Algorithms in Synthesis of Approximate Circuits**<br>*Lida Kouhalvandi:* **Optimizations for Improving Efficiency-Accuracy of Approximate Computing Circuits**<br>*Douglas Rossi de Melo:* **Interconnection Architecture for Dependable Multicore Systems**<br>*Alexandra Zimpeck:* **Reliability-Oriented Approaches to Mitigate Process Variations and Soft Errors on FinFET Technologies**<br>*Florenc Demrozi:* **Virtual Coaching for Assisting Activities of Daily Life**<br>*Alessandro Danese:* **System-level functional and extra-functional characterization of SoCs through assertion mining**<br>*Anastasis Keliris:* **Automating Cybersecurity Studies of Industrial Control Systems (**)**<br>*Vijender Kumar Sharma :* **Nonlinear Modeling and Analysis of Power Delivery Network using Volterra Series**<br>*Abhijit Das :* **Optimising NoC in Many-Core Systems**<br>*Muhammad Awais:* **Design Space Exploration for Approximate Circuits Synthesis**<br>*Debjyoti Bhattacharjee:* **Synthesis, Technology mapping and Optimization for Emerging Technologies**<br>*Freddy Forero:* **New Defect Model for Interconnect Open Defect in FinFET Digital Gates**<br>*Zahira Perez Rivera:* **An optimization algorithm of circuit performance under local intra-die process variations** | |
| 15.30-16.00 | Coffee break | |
| 16.00-17.00 | **Session 2**: Digital architectures: NoC, multi- and many-core, hybrid, and reconfigurable<br>*Chair: Ian O'Connor (Univ. Lion, France)*<br>Room: Sala Mascagni | **Session 3**: Prototyping, verification, modeling, and simulation: from digital to analog circuits<br>*Chair: Katell Morin-Allory (Univ. Grenoble-Alpes, France)*<br>Room: Sala Ponchielli |
| | 16.00 - *Simi Zerine Sleeba, John Jose, Maurizio Palesi, Rekha K. James and Mini Nair.* **Traffic Aware Deflection Rerouting Mechanism for Mesh Network on Chip (*)**<br>16.20 - *Evelina Forno, Andrea Acquaviva, Yuki Kobayashi, Enrico Macii and Gianvito Urgese.* **A Parallel Hardware Architecture For Quantum Annealing Algorithm Acceleration**<br>16.40 - *Shahzad Muzaffar and Ibrahim Elfadel.* **An Instruction Set Architecture for Low-power, Dynamic IoT Communication** | 16.00 - *Ernesto Sanchez, Pasquale Davide Schiavone, Annachiara Ruospo, Francesco Minervini, Florian Zaruba, Germain Haugou and Luca Benini.* ***An Open-Source Verification Framework for Open-Source Cores: A RISC-V Case Study***<br>16.20 - *Utkarsh Gupta, Irina Ilioaea, Vikas Rao, Arpitha Srinath, Priyank Kalla and Florian Enescu.* **On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields (*)**<br>16.40 - *Naoki Ojima, Toru Nakura, Tetsuya Iizuka and Kunihiro Asada.* **A Synthesizable Digital Low-Dropout Regulator Based on Voltage-to-Time Conversion (*)** |
| 17.00-17.30 | Transfer to city tour (1st meeting point: hotel lobby) | |
| 17.30-19.30 | City tour (2nd meeting point: Vittorio Emanuele statue - Piazza Bra) | |
| 19.30-21.30 | Welcome reception: Pizzeria Corte Farina | |

# Tuesday, October 9th

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| 9.00-9.30 | **Registration** | |
| 9.30-10.30 | **Keynote** - Valeria Bertacco (University of Michigan, USA): Re-imagining scalable system design<br>*Chair: Masahiro Fujitsa (Univ. Tokyo, Japan)*<br>Room: Sala Mascagni | |
| 10.30-11.00 | Coffee break | |
| 11.00-12.20 | **Session 4**: Variability, reliability, and test<br>*Chair: Matteo Sonza Reorda (Politecnico di Torino, Italy)*<br>Room: Sala Mascagni | **Session 5**: Hardware security<br>*Chair: Lilian Bossuet (Univ. St. Etienne, France)*<br>Room: Sala Ponchielli |
| | 11.00 - *Riccardo Cantoro, Sara Carbonara, Andrea Floridia, Ernesto Sanchez, Matteo Sonza Reorda and Jan-Gerd Mess:* **An analysis of test solutions for COTS-based systems in space applications (*)** | 11.00 - *Suyuan Chen and Ranga Vemuri:* **On the Effectiveness of the Satisfiability Attack on Split Manufactured Circuits** |
| | 11.20 - *Andrés Felipe Gómez, Freddy Forero, Victor Champac and Kaushik Roy:* **Robust Detection of Bridge Defects in STT-MRAM Cells Under Process Variations (*)** | 11.20 - *Konstantin Braun, Tim Fritzmann, Georg Maringer, Thomas Schamberger and Johanna Sepulveda.* **Secure and Compact Full NTRU Hardware Implementation** |
| | 11.40 - *Leonardo H. Brendler, Alexandra L. Zimpeck, Cristina Meinhardt and Ricardo Reis.* **Evaluating the Impact of Process Variability and Radiation Effects on Different Transistor Arrangement** | 11.40 - *Ming Ming Wong, Vikramkumar Pudi and Anupam Chattopadhyay:* **Lightweight and High Performance SHA-256 using Architectural Folding and 4-2 Adder Compressor** |
| | 12.00 - *Zahira Perez, Hector Villacorta and Victor Champac:* **An accurate novel gate-sizing metric to optimize circuit performance under local intra-die process variations.** | 12.00 - *Anastasis Keliris, Charalambos Konstantinou, Marios Sazos and Michail Maniatakos:* **Low-budget Energy Sector Cyberattacks via Open Source Exploitation (*)** |
| 12.20-13.30 | Lunch | |
| 13.30-14.30 | **Session 6**: Machine learning and emerging technologies for low-power and energy efficienc SoC design<br>*Chair: Mirko Loghi (Univ. Udine, Italy)*<br>Room: Sala Mascagni | **Special session 2**: Design understanding<br>*Chair: Heinz Riener (EPFL, Switzerland)*<br>Room: Sala Ponchielli |
| | 13.30 - *Edouard Giacomin and Pierre-Emmanuel Gaillardon.* **Differential Power Analysis Mitigation Technique Using Three-Independent-Gate Field Effect Transistors** | 13.30 - *Gianluca Martino, Gorschwin Fey:* **Advantages of automatic generation and selection of temporal-logic properties** |

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| | 13.50 - *Valentino Peluso and Andrea Calimera.* **Energy-Driven Precision Scaling for Fixed-Point ConvNets (*)**<br><br>14.10 - *Osman Elgawi.* **Pipelined Machine Learning Accelerator Implemented on FPGA** | 13.50 - *Tara Ghasempouri, Jaan Raik:* **An improvement of assertion-based verification: How can assertions be more readable?**<br>14.10 - *Swen Jacobs:* **System specifications and environment assumptions in reactive synthesis** |
| 14.30-16.00 | **Panel session**: Computation-in-memory: Hype or Hope?<br><br>*Moderator: Said Hamdioui (TU Delft)*<br>Room: Sala Mascagni | |
| | Panelists:<br><br>Ian O'Connor (Univ. Lyon, France)<br><br>Mehdi Tahoori (Karlsruhe Institute of Technology, Germany)<br><br>Henri-Pierre Charles (CEA, France)<br><br>Lionel Torres (Lirmm, France) | |
| 16.00-16.30 | Coffee break | |
| 16.30-22.00 | Wine tour + Gala dinner (Meeting point: hotel lobby) | |

## Wednsday, October 10th

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| 9.00-9.30 | **Registration** | |
| 9.30-10.30 | **Keynote** - Heinz Koeppl (TU Darmstadt, Germany): Computational challenges in the design automation for synthetic biology<br><br>*Chair: Manfred Glesner (TU Darmstadt, Germany)*<br>Room: Sala Mascagni | |
| 10.30-11.00 | Coffee break | |
| 11.00-12.20 | **Special session 3**: Neuromorphic computing - from robust hardware architectures to testing strategies<br>*Chair: Lorena Anghel (Univ. Grenoble-Inp, France)*<br>Room: Sala Mascagni | **Special session 4**: Non-volatile emerging memories - breaking down the memory wall<br><br>*Chair: Lionel Torres (Lirmm, France)*<br><br>Room: Sala Ponchielli |
| | 11.00 - *Benoît Miramond:* **Neuromorphic architectures, a bridge between machine learning and brain-inspired computing** | 11.00 - *Ian O'Connor, Mayeul Cantan, Cédric Marchand, Bertrand Vilquin, Bastien Giradu, Jean-Philippe Noël, Stefan Slesazeck, Evelyn Breyer, Thomas Mikolajick, Adrian Ionescu and Igor Stolichnov.* **Prospects for energy-efficient edge computing with integrated HfO2-based ferroelectric devices** |

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| | 11.15 - *Elisa Vianello:* **Phase Change Memory and Metal Oxide Resistive Memory as Artificial Synapses in Spiking Neural Networks**<br><br>11.30 - *Elena-Ioana Vatajelu:* **On the Design of Spiking Neural Nerworks**<br><br>11.45 - *Lorena Anghel:* **Robustness of Spiking Neural Networks**<br><br>12:00 - *Giorgio DiNatale:* **Testability Aspects of Spiking Neural Networks** | 11.20 - *Erya Deng, Zhaohao Wang, Wang Kang, Shaoqian Wei and Weisheng Zhao.* **Multi-bit nonvolatile flip-flop based on NAND-like spin transfer torque MRAM**<br><br>11.40 - *Sophiane Senni, Frederic Ouattara, Jad Modad, Kaan Sevin, Guillaume Patrigeon, Pascal Benoit, Pascal Nouet, Lionel Torres, François Duhem, Gregory Di Pendina and Guillaume Prenat.* **From Spintronic Devices to Hybrid CMOS/Magnetic System On Chip**<br>12.00 - *Mathieu Moreau, Eloi Muhr, Marc Bocquet, Jean-Michel Portal, Bastien Giraud, Hassen Aziza, Jean-Philippe Noel and Henri-Pierre Charles.* **Reliable ReRAM-based logic operations for computing in memory** |
| 12.20-13.30 | Lunch | |
| 13.30-14.30 | **Session 7**: Embedded and cyberphysical systems: architecture, design, and software<br>*Chair: Fatih Ugurdag (Ozyegin Univ., Turkey)*<br>Room: Sala Mascagni | **Session 8**: CAD: Synthesis and analysis<br>*Chair: Viktor Kravetz (IBM, USA)*<br>Room: Sala Ponchielli |
| | 13.30 - *Stefano Aldegheri, Silvia Manzato and Nicola Bombieri.* **Enhancing Performance of Computer Vision Applications on Low-Power Embedded Systems Through Heterogeneous Parallel Programming**<br><br>13.50 - *Luiz Antonio De Oliveira Junior and Edna Barros.* **An FPGA-based Hardware Accelerator for Scene Text Character Recognition**<br><br>14.10 - *Rahul Shrestha and Ashutosh Sharma.* **VLSI-Architecture of Radix-2/4/8 SISO Decoder for Turbo Decoding at Multiple Data-rates** | 13.30 - *Anna Bernasconi, Antonio Boffa, Linda Pagli and Fabrizio Luccio.* **Two Combinatorial Problems on the Layout of Switching Lattices**<br><br>13.50 - *Luca Stornaiuolo, Marco Rabozzi, Marco Domenico Santambrogio, Donatella Sciuto, Giulio Stramondo, Catalin Bogdan Ciobanu and Ana Lucia Varbanescu:* **HLS Support for Polymorphic Parallel Memories**<br>14.10 - *Valerio Tenace and Andrea Calimera.* **Inferential Logic: a Machine Learning Inspired Paradigm for Combinational Circuits** |
| 14.30-16.00 | **Poster session**<br><br>*Chair: Alessandro Danese (Univ. Verona, Italy)*<br>Room: Foyer | |
| | *Kaori Matsumoto, Tetsuya Hirose, Hiroki Asano, Yuto Tsuji, Yuichiro Nakazawa, Nobutaka Kuroki and Masahiro Numa:* **An ultra-low power active diode using a hysteresis common gate comparator for low-voltage and low-power energy harvesting systems**<br><br>*Mubashir Hussain and Hui Guo:* **A Bandwidth-Aware Authentication Scheme for Packet-Integrity Attack Detection on Trojan Infected NoC** | |

*Serhiy Avramenko, Massimo Violante, Siavoosh Payandeh Azad, Behrad Niazmand, Maksim Jenihhin and Jaan Raik:* **Upgrading QoSinNoC: Efficient Routing for Mixed-Criticality Applications and Power Analysis**

*Anna Bernasconi, Valentina Ciriani and Luca Frontini:* **Testability of Switching Lattices in the Stuck at Fault Model**

*Muhammad Awais, Hassan Ghasemzadeh Mohammadi and Marco Platzner:* **An MCTS-based Framework for High-Level Synthesis of Approximate Circuits**

*Steve Bigalke and Jens Lienig:* **FLUTE-EM: Electromigration-Optimized Net Topology Considering Currents and Mechanical Stress**

*Keerthikumara Devarajegowda and Wolfgang Ecker:* **Meta-model Based Automation of Properties for Pre-Silicon Verification**

*Stefano Centomo, Marco Panato and Franco Fummi:* **Cyber-physical Systems Integration in a Production Line Simulator**

*Yakup Murat Mert:* **Key Architectural Optimizations for Hardware Efficient JPEG-LS Encoder**

*Florenc Demrozi, Kevin Costa, Federico Tramarin and Graziano Pravadelli:* **A graph-based approach for mobile localization exploiting real and virtual landmarks**

*Mahdi Tala and Davide Bertozzi:* **Understanding the design space of wavelength-routed optical NoC topologies for energy-per-bit optimization**

*Mahabub Hasan Mahalat, Nikhil Ugale, Rohit Shahare and Bibhash Sen:* **Design of Latch based Configurable Ring Oscillator PUF targeting Secure FPGA**

*Gionata Benelli, Gabriele Meoni and Luca Fanucci:* **A low power keyword spotting algortihm for memory constrained embedded systems**

15.30-16.00 Coffee break

16.00-16.30 **Award ceremony - closing remarks**

Room: Sala Mascagni

* Best Paper Candidate

** PhD contribution scheduled during the poster session on wed 10 at 2:30pm, due to unavailability of the speaker on Mon 8